NOTICE

Campus Drive for BE & ME/M.Tech– 2018 pass out batch

A leading core electronics semi conductor & Chip designing Multi National Company i.e **PerfectVIPs** ,having headquartered in heart of Silicon Valley, San Jose, California, USA and in India they have operations at Ahmedabad, Bhuwneshwar and Bangalore has given consent for pool campus drive for 2018 batch of **BE/B.Tech & ME/M.Tech (EC & EX/EEE)**

About the Company: Founded in **2010**, PerfectVIPs is empowering the chip design industry by providing highest quality Verification IP products for Storage applications, Peripheral interconnects and On-Chip bus interfaces.
PerfectVIPs products accelerate the chip design & verification cycle with higher reliability and lower risk and cost.To provide robust verification for many interface protocol based designs that reduces design time, design risk and cost of verification, PerfectVIPs has several Verification-IPs called Genie VIPs.PerfectVIPs provides world's largest portfolio of verification IP solutions like PCI-express 3.0,PCI-express 2.0/1.1, USB 3.0, USB 2.0, Ethernet, SPI, AMBA (AHB, APB, & AXI), SMBus, OCP, SAS, SATA, ONFI and Fibre Channel.
Each Genie VIP consists of: Bus Functional Model, Protocol Monitor,Checker, comprehensive compliance Test Suite,API,control knobs,error injectors and call back features. All are fully developed in native System Verilog , family of VIPs having flexibility to work with popular languages like VHDL,Verilog,Vera,system C,C++ and 'e' and on all commonly used simulators and platforms. Company URL- http://www.perfectvips.com/

Solutions and Products for IP / SOC / ASIC / FPGA

Technologies for Industries: Storage / Automotive / IOT / Networking / Wireless & Mobile / Consumer / Aerospace & Defence

Job Description:

	BE/B Tech(UG)	**ME/M.Tech (PG)**
Branch	EC & EX/EEE	EC & EX/EEE
Criteria	65% throughout	65% throughout
Batch	2017 and 2018	2017 and 2018
Profile	Trainee Engineer	Software Engineer
Package	1.80- 3.00 LPA	2.20- 4.00 LPA
Working Days	Monday to Friday	
Job Location	Bangalore / Ahmedabad	
Date of Campus	26/06/2018	
Reporting time	9:30 A.M.	
Venue	Civil Auditorium, MIT, Ujjain (M.P)	

Selection Process: PPT
Online Test (01 Hours, No Negative Marking)
Technical Interview & Personal Interview

Skills Required:
C, C++, Digital Electronics concepts
Include Verilog / VHDL / System Verilog in case of VLSI stream
Based on subject covered in VLSI they may have knowledge on Verilog
Knowledge of VHDL
Knowledge of System Verilog

For VLSI knowledge of UVM is plus
Should Understand Verilog Design
Must have good spoken and written communication skills
Collaborate well in a team